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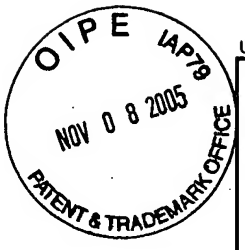

PTO/SB/21 (09-04)
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/698,257
Filing Date	October 30, 2003
First Named Inventor	William W. CHENG
Art Unit	2816
Examiner Name	K. B. Wells
Attorney Docket Number	535352003600

Total Number of Pages in This Submission

ENCLOSURES (*Check all that apply*)

- [x] Fee Transmittal Form
- [ ] Fee Attached
- [ ] Amendment/Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
- [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	MORRISON & FOERSTER LLP (CN 25224)		
Signature			
Printed name	David T. Yang		
Date	November 8, 2005	Reg. No.	44,415

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV 506673825US, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: November 8, 2005 Signature: _____ (Marco Jimenez)

PTO/SB/17 (12-04v2)
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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	10/698,257
Filing Date	October 30, 2003
First Named Inventor	William W. CHENG
Examiner Name	K. B. Wells
Art Unit	2816
Attorney Docket No.	535352003600

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 03-1952 Deposit Account Name: Morrison & Foerster LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fees Paid ($)**
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 =	_____	x _____	= _____

Multiple Dependent Claims	
Fee ($)	**Fee Paid ($)**
_____	_____

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 =	_____	x _____	= _____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ /50	_____ (round up to a whole number) x	_____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): 1402 Filing a brief in support of an appeal	500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent)	44,415	Telephone	(213) 892-5587
Name (Print/Type)	David T. Yang			Date	November 8, 2005

Docket No.: 535352003600
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
CHENG et al.

Application No.: 10/698,257

Filed: October 30, 2003

Art Unit: 2816

For: DIGITAL-TO-ANALOG CONVERTER WITH ALWAYS-ON CASCODE TRANSISTORS

Examiner: K.B. Wells

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on October 5, 2005 and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2), and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

11/14/2005 WABDELR1 00000040 031952 10698257
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This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is TelASIC Communications, Inc., the current assignee of the above application.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Current Status of Claims

1. Claims canceled: 1-27, 30-32, 34, 36, and 40

2. Claims withdrawn from consideration but not canceled: none

3. Claims pending: 28, 29, 33, 35, 37, 38, and 39

4. Claims allowed: none

5. Claims rejected: 28, 29, 33, 35, 37, 38, and 39

B. Claims on Appeal

The claims on appeal are claims 28, 29, 33, 35, 37, 38, and 39, of which Claim 28 is an independent claim.

IV. STATUS OF AMENDMENTS

Applicant did not file any amendments in response to the rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to a high speed, high resolution digital to analog converter (DAC).

With reference to Fig. 3 of the present application, a plurality of cascode current output block 52 is used as a unitary switching element (e.g., a unit cell) of a DAC. This is in contrast to the conventional differential pair switching element such as 12 and 14 shown in the DAC of Fig. 1 of the present application.

In accordance with the present invention, the cascode current switch cells employ trickle currents that are placed at the outputs of the switching transistors to keep the cascode transistors in the switching path on a constant "on" state, thereby decreasing the "switching time" and settling time of the switching transistors, as well as decrease the parasitic capacitance associated with the conventional uncascoded switching elements. In addition, the use of the cascode current switches in a DAC environment provides isolation between the switching transistors and the output summing nodes, thereby further improving the accuracy and dynamic range of the DAC.

A. Summary of Claimed Subject Matter in Independent Claim 28

Claim 28 is directed generally to Fig. 3 of the present application. Specifically, Claim 28 recites a DAC having a first and second summing bus (e.g., 16 & 18 in Fig. 3), a plurality of current switch cells (e.g., 52), each of which includes a first current source (e.g., 20 in Fig. 3) for supplying a first current, a pair of differential transistors (e.g., Q1 & Q2 in Fig. 3), a pair of cascode transistors (e.g., Q_A and Q_B in Fig. 3) having emitters respectively coupled to the collectors of Q1 and Q2 and collectors coupled to the first and second summing buses, and two additional current sources for supplying trickle currents to the emitters of the cascode transistors (e.g., 56 & 58 in Fig. 3).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 28, 29, 33, 35, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baskett (U.S. patent no. 6,333,672) in view of applicant's admitted prior art.

Claims 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baskett.

VII. ARGUMENT

As discussed above, Claim 28 is directed to a digital-to-analog circuit employing a plurality of current switches that include a cascode circuit having supplied thereto trickle current at the outputs of the switching transistors. By implementing the cascode circuits with trickle currents, the switching time of the transistors can be reduced, and parasitic capacitance (and hence the Miller Effect) can be reduced or eliminated. As recited in Claim 28, the multiple unit cells are summed together into a load resistor to make up a high-resolution DAC. The use of the cascode circuits with trickle currents as unit cells in a DAC improves the performance of the DAC by providing a faster overall operating speed and improved accuracy, while eliminating parasitic capacitance (a.k.a. Miller effect) typically associated with convention DAC architecture using transistors that do not apply the principle of using trickle currents.

The Primary Examiner rejected Claims 28, 29, 33, 35, and 37 under 35 U.S.C. 103(a) as being unpatentable over Baskett (U.S. patent no. 6,333,672) in view of applicant's admitted prior art (specifically, Fig. 1 of the present application), and rejected Claims 38 and 39 as being unpatentable over Baskett alone.

First, Applicants note that Baskett does not contain any disclosure or suggestion of a digital-to-analog converter. Rather, Baskett is directed to a differential digital logic gate having two different states of digital outputs. Secondly, Baskett does not contain any disclosure or teaching of

using multiple units of current cells for switching purposes. The Primary Examiner does not expressly disagree with the two above points. Rather, the Primary Examiner states that it is obvious to incorporate the current switch of Fig. 1 in Baskett into a convention DAC, and that such a combination teaches the invention claimed by Claim 28. Specifically, the Primary Examiner states:

> "As to claims 28-30, these claims recite the same limitations as claims 1-22, except in a D/A converter having plural switches, each with the details of claims 1-22. Applicant admits on page 2 of the instant application that it is known in the art the selectively switch plural current sources into or out of a current summing device. Using the Baskett Fig. 1 logic circuit as such as switch would have been obvious to those having ordinary skill in the art, the motivation for using the same Fig. 1 logic circuit as the driver stage being to obtain the benefits taught by Baskett, i.e., to obtain the advantage of reduced switching delays associated with the Fig. 1 circuit, see column 1, lines 40-45 of Baskett." (Office Action mailed on November 16, 2004, at page 5).

Applicants respectfully submit that the Primary Examiner's combination of page 2 of the present application and Fig. 1 of Baskett is improper and is not supported by well-established patent law.

First, it should be noted that the discussions on page 2 of the present application provides the inventors' observation of some of the disadvantages of the conventional DACs (such as the convention DAC shown in Fig. 1 of the present application). The discussions contained on page 2 of the present application, though is with respect to conventional DACs, is of course not prior art itself.

Secondly, and more importantly, there is no teaching, suggestion, or motivation for combining Fig. 1 of Baskett with the admitted prior art. Specifically, there is no motivation for combining circuitry of a differential logic gate, used for digital output purposes and having only two digital outputs of high and low, into a circuitry of multiple switching cells for outputting analog

outputs of various resolutions. Applicants respectfully submit that any such combination is in hindsight of the present application.

As it is well known in the art, there exist many different types of current switches in electrical applications, just as there exist numerous different electrical elements generally. It is well recognized that a novel combination of elements, even if the elements are known in the art, is patentable. See, e.g., In re Lunsford, 357 F.2d 380, 384 (C.C.P.A. 1966) (citing In re Wright, 268 F.2d 757 (C.C.P.A. 1959). At the same time, it is also well settled patent law that hindsight cannot be used as motivation for combining prior art references. See, e.g., Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1139 (Fed. Cir. 1985) (vacating judgment by trial court, noting it is error to reconstruct the patentee's claimed invention from the prior art by using the patentee's claim as a "blueprint.") (citing Kalman v. Kimberly-Clark Group, 713 F.2d 760, 774 (Fed. Cir. 1983), cert denied 465 U.S. 1026 (1984)). Rather, there must exist some suggestion, teaching, or motivation that would have led a person of ordinary skill in the art to combine the prior art references in a manner claimed. See Graham v. John Deere Co., 383 U.S. 1 (1966); In re Dembiczak, 175 F.3d 994, 998 (Fed. Cir. 1999). To do otherwise, "combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability -- the essence of hindsight." Dembiczak, 175 F.3d at 999. In this regard, the Federal Circuit has consistently held that a person of ordinary skill in the art "must not only have had some motivation to combine the prior art teachings, but some motivation to combine the prior art teachings in the particular manner claimed." Teleflex Inc. v. KSR Int'l Co., 119 Fed. Appx 282 (Fed. Cir. 2005) (citing In re Kotzab, 217 F.3d 1365, 1371 (Fed. Cir. 2000) ("Particular findings must be made as to the reason the skilled artisan, with no

knowledge of the claimed invention, would have selected these components for combination in the manner claimed.")).

In this instance, the Examiner points to column 1, lines 40-45 of Baskett for combining Baskett and the admitted prior art. Column 1, lines 40-45 of Baskett states:

> "Referring to FIG. 1, an improved prior art differential logic circuit 10 is illustrated which provides one method of reducing switching delays induced by toggling the conduction states of differential input transistor pairs by using cascode amplifiers."

The above language from Baskett merely describes the general characteristics of a particular type of differential logic circuit. The cited language makes no reference whatsoever to a digital-to-analog converter or a current summing device. In fact, the circuitry of Fig. 1 in Baskett is discussed only within the context of digital output applications wherein the outputs are purely digital (e.g., a high and a low output) (see column 1, line 12 to column 2, line 7); there is no suggestion, teaching, or motivation of any kind from that statement, or from any disclosure of Baskett, for combining the circuitry with an analog output circuit (such as a DAC) that produces multiple output states as it is claimed by the currently pending claims.

Other than the above-cited language from Baskett, the Primary Examiner does not point to any suggestion or teaching, explicit or implicit, that can be found in the admitted prior art, Baskett, or the knowledge of those of ordinary art for combining the references in a manner claimed by the pending claims. Rather, the Primary Examiner simply remarks that motivation being "to obtain the advantage of reduced switching delays associated with the Fig. 1 circuit (of Baskett)," when in fact it wouldn't make any sense, from a digital logic perspective as taught by Baskett, to construct multiple [>2] logic states. Indeed, the Primary Examiner appears to have used the claims as a foundational blueprint and, in hindsight, reconstructed the claimed invention by selectively

combining the references. Accordingly, Applicants respectfully appeal the Primary Examiner's final rejection and submit that the combination of the admitted prior art and Baskett is improper, and that Claims 28, 29, 33, 35, and 37, as well as dependent Claims 38 and 29, are not unpatentable over the two references.

Additional dependent claims, such as Claim 33, includes subject matter that are in of it themselves patentably distinguishable from Baskett and the admitted prior art. In particular, Baskett does not teach or suggest a buffer transistor connected between the first current source (e.g., 20 in Fig. 3 of the present application) and the common emitters of the differential pair of transistors Q1 and Q2.

Similarly, with respect to Claims 38 and 39, which the Primary Examiner also rejected Claims 38 and 39 as being obvious in view of Baskett, Applicants respectfully submit that Baskett simply does not suggest any of the additional limitations recited in dependent Claims 38 and 39 of the present application.

In view of the above, Applicant respectfully appeals from the Examiner's rejection in the Final Office Action and again in the Advisory Action.

VIII. CLAIMS APPENDIX

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE APPENDIX

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the Examiner is being submitted.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings are referenced above, hence no Appendix is included.

Dated: November 8, 2005

Respectfully submitted,

By _____
David T. Yang
Registration No.: 44,415
MORRISON & FOERSTER LLP
555 West Fifth Street
Los Angeles, California 90013-1024
(213) 892-5587

APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/698,257:

Claims 1-27 (canceled)

Claim 28 A digital to analog converter comprising:

a first current summing bus;

a second current summing bus; and

a plurality of current switches, each switch including:

a first current source for supplying a first current;

a differential pair of transistors adapted to couple said first current to either the first current summing bus or the second current summing bus in response to a pair of complementary input signals;

a pair of cascode transistors having emitters respectively coupled to the collectors of said differential pair of transistors, and collectors coupled to said first and second current summing buses, respectively; and

second and third current sources adapted to respectively supply first and second trickle currents to the emitters of said pair of cascode transistors in order to maintain said pair of cascode transistors in an 'on' state regardless of the states of said differential pair of transistors,

wherein the trickle currents are approximately 10 to 100 times smaller than said first current.

Claim 29 The invention of Claim 28 wherein the bases of said pair of cascode transistors are connected in common to a voltage potential.

Claims 30-32 (canceled)

Claim 33 The invention of Claim 28 wherein each current switch further includes a buffer transistor connected between said first current source and the common emitters of differential pair of transistors.

Claim 34 (canceled)

Claim 35 The invention of Claim 28 wherein said first and second trickle currents are approximately equal.

Claim 36 (canceled)

Claim 37 The invention of Claim 28 wherein each current switch further includes a driver circuit for supplying said pair of complementary input signals.

Claim 38 The invention of Claim 37 wherein said driver circuit includes:

a fourth current source for supplying a fourth current;

a second differential pair of transistors adapted to couple said fourth current to one of the collectors of said second differential pair of transistors in response to a second pair of complementary input signals;

a second pair of cascode transistors having emitters respectively coupled to the collectors of said second differential pair of transistors;

fifth and sixth current sources adapted to respectively supply third and fourth trickle currents to the emitters of said second pair of cascode transistors in order to maintain said second pair of cascode transistors in an 'on' state regardless of the states of said second differential pair of transistors; and

two transistors having bases respectively coupled to the collectors of said second pair of cascode transistors and emitters adapted to output said pair of complementary input signals.

Claim 39 The invention of Claim 38 wherein said fourth current and said third and fourth trickle currents are chosen to generate a low output voltage swing at the emitters of said two transistors having bases respectively coupled to the collectors of said second pair of cascode transistors.

Claim 40 (canceled)